CS5101AN/D

Secondary Side Post Regulator (SSPR) for Switching Power Supplies with Mulitple Outputs

ON Semiconductor™

http://onsemi.com

APPLICATION NOTE

This application note describes the common post regulation methods used in power supply design and introduces the CS5101 Secondary Side Post Regulator Control IC. It also shows a detailed design example of a dual output, current mode control, forward converter using the CS3842A and CS5101 controllers.

Introduction

In Switch Mode Power Supplies (SMPS) a transformer provides isolation between the primary source and the secondary load(s). If the SMPS controller is located on the primary side of the transformer, the feedback voltage from the secondary is fed back to the primary side through another isolation barrier, usually an opto coupler.

Tight output regulation is more difficult in multiple output power supplies. The following are the most popular techniques.

1. The Linear Regulator, Figure 1, is the simplest and the most popular for low current (3.0 A) applications. The major disadvantage of the linear regulator is its poor efficiency.
2. A Step–Down Buck Regulator, Figure 2, can be used as a post regulator. Efficiencies up to 90% can be achieved by using this method. This solution looks very attractive in the low and medium power range (3.0 A to 8.0 A). However, several additional high cost components are required, including, a power switch, inductor and capacitors.
3. A Magnetic Amplifier Post Regulator, Figure 3, offers high efficiency and tight regulation for output currents greater than 5.0 A .

   Its drawbacks include: the difficulty in implementing overcurrent protection, poor regulation characteristics at light or no load conditions and the cost of the high frequency (200 kHz) magnetic amplifier inductor.
4. A Secondary Side Post Regulator (SSPR), Figure 4, uses a semiconductor switch with either leading edge (delayed turn–on) or trailing edge (delayed turn–off) modulation.

   An SSPR provides excellent regulation, high efficiency, high frequency operation, lossless overcurrent protection and remote ON/OFF control.

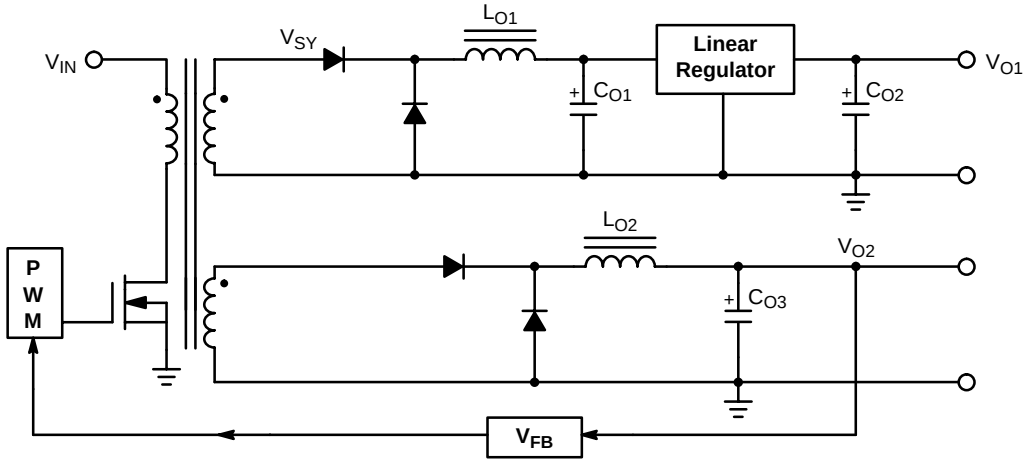

Figure 1. Linear Regulator

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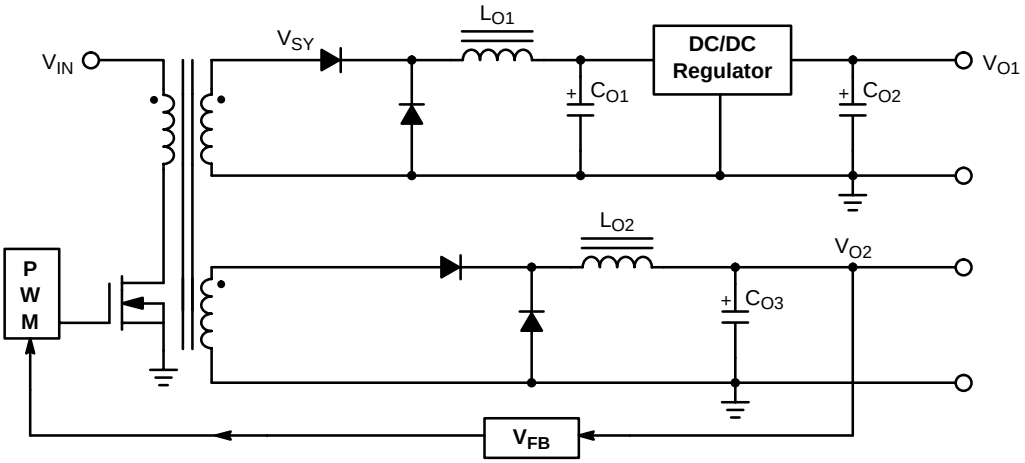

Figure 2. Switching Post Regulator

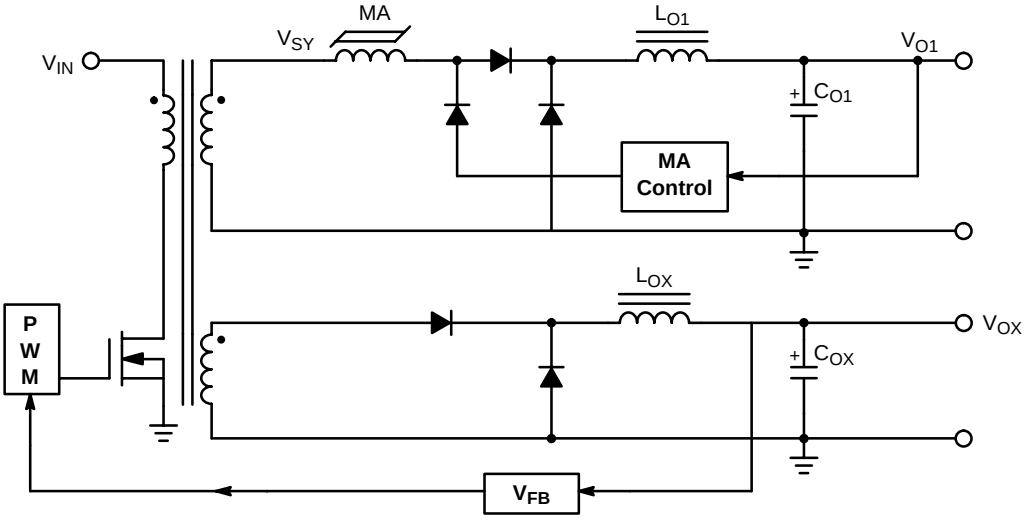

Figure 3. MAGAMP

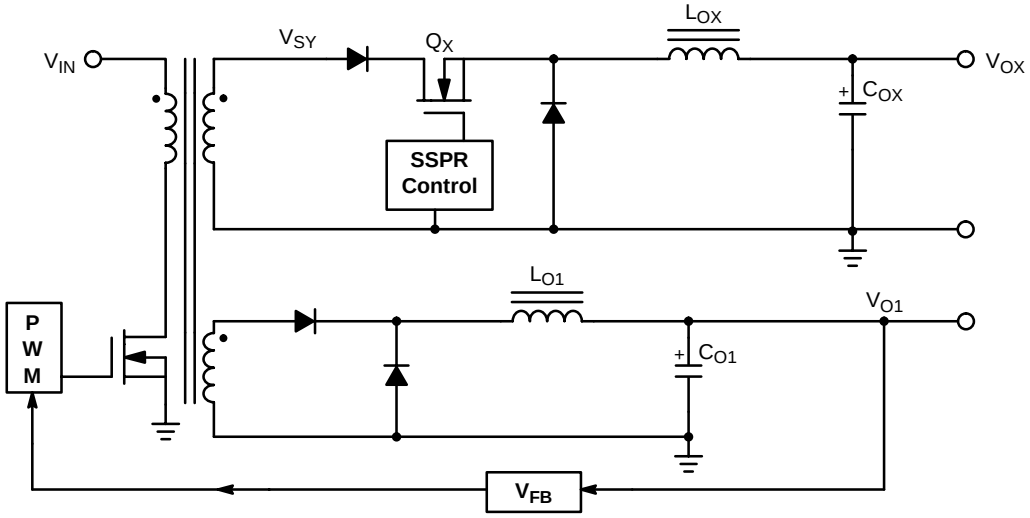

Figure 4. SSPR

SSPR Operation

An SSPR regulator allows the designer to build multiple output power supplies with each output individually controlled without any feedback to the primary side.

The SSPR switch is connected in series with the secondary side rectifier and output inductor.

In a forward converter topology using current mode control, the primary controller maintains a constant volt–second product. The primary side current waveforms for both leading edge and trailing edge operation are shown in Figure 5. There is a step change in the primary current when the SSPR turns on, or turns off. Trailing edge modulation will cause loop instability in current mode control using peak current sensing. This is not a problem with voltage mode control regulators. Leading edge modulation does not have this limitation.

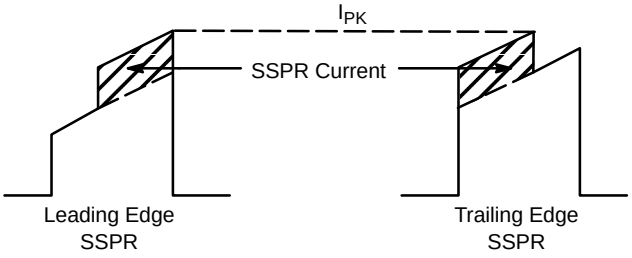

Figure 5. Primary Switch Current Waveforms

The CS5101 SSPR from ON Semiconductor Corporation is designed for leading edge modulation and is compatible with both voltage and current mode control.

CS5101 Functional Pin Description

Pin Symbol	Function
SYNC	Frequency synchronization input.
V_{CC}	Logic supply (8.0 V to 45 V).
V_{REF}	5.0 V output voltage reference.
LGND	Logic level ground (analog and digital ground tied).
V_{FB}	Inverting input providing feedback through error amplifier.
COMP	Error amplifier output and compensation pin.
RAMP	Programmable ramp input.
IS+	Noninverting input for current sense amplifier.
IS–	Inverting input for current sense amplifier.
IS COMP	Compensation pin for current sense amplifier.
PGND	Power ground.
V_G	Gate drive for output stage.
V_C	Collector for output power stage.
V_D	DRAIN connection for external FET.
AGND	Analog ground.
DGND	Digital ground.

A block diagram of the CS5101 SSPR is shown in Figure 6. When the voltage at the V_{CC} pin is below the start–up threshold, the output stage is low and the external power switch (usually an N–FET) is off. The output stage is disabled until the V_{CC} voltage and V_{REF} are within specification.

The switching cycle begins when the synchronization voltage at the SYNC pin exceeds 2.5 V. This synchronization signal is derived from the voltage on the secondary side of the transformer. The ramp capacitor connected to the RAMP pin charges towards 3.5 V. The capacitor voltage is compared to the buffered control voltage, V_C by the PWM comparator C1. When the ramp capacitor voltage exceeds the V_C voltage, the output of C1 goes high and turns on the external power switch connected to V_G. As C1 goes high it also sets flip–flop F1 which latches the output. During the trailing edge of the pulse, the ramp capacitor is discharged. The output stage turns off only on the trailing edge of the synchronization pulse when the voltage at the SYNC and RAMP pins are below the thresholds of comparators C2 and C4 respectively. G2 resets the flip–flop F1.

The error amplifier, EA, monitors the output voltage and compares it to an internal 2.0 V reference. The buffer amplifier inverts the error signal and applies it to the input of C1.

The current sense amplifier, IS, monitors the output current. During normal operation the output of IS is high and the diode is reverse biased. When the overcurrent threshold is exceeded, the output goes low, the diode is forward biased and the current sense amplifier sinks current from the error amplifier. This pulls the error amplifier output low and shuts off the output stage through G3.

Since all three pins of the differential amplifier are accessible, high side or low side current sensing is possible. The circuit is designed so that the current sense amplifier is guaranteed to sink more current than the error amplifier, EA, can source.

The external power switch is driven by a grounded totem–pole output stage. The output stage remains off until the output of C1 goes high. Since the external power switch turns off on the trailing edge of the secondary pulse, lossless turn–off is achieved. If the output controlled by the SSPR is shut down or disabled while the main output is still operational, a DC voltage equal to a peak secondary voltage will build up at the drain of the power switch. The drain pin V_D monitors this voltage and keeps the output stage off, even if the supply voltage, V_{CC}, disappears. The output stage remains off as long as any abnormal conditions exist. If normal operating conditions are restored while there is no synchronization pulse, the controller will process the next available pulse. If normal operating conditions are restored during a pulse, the rest of the pulse is ignored and the controller will resume the normal operation at the rising edge of the next pulse.

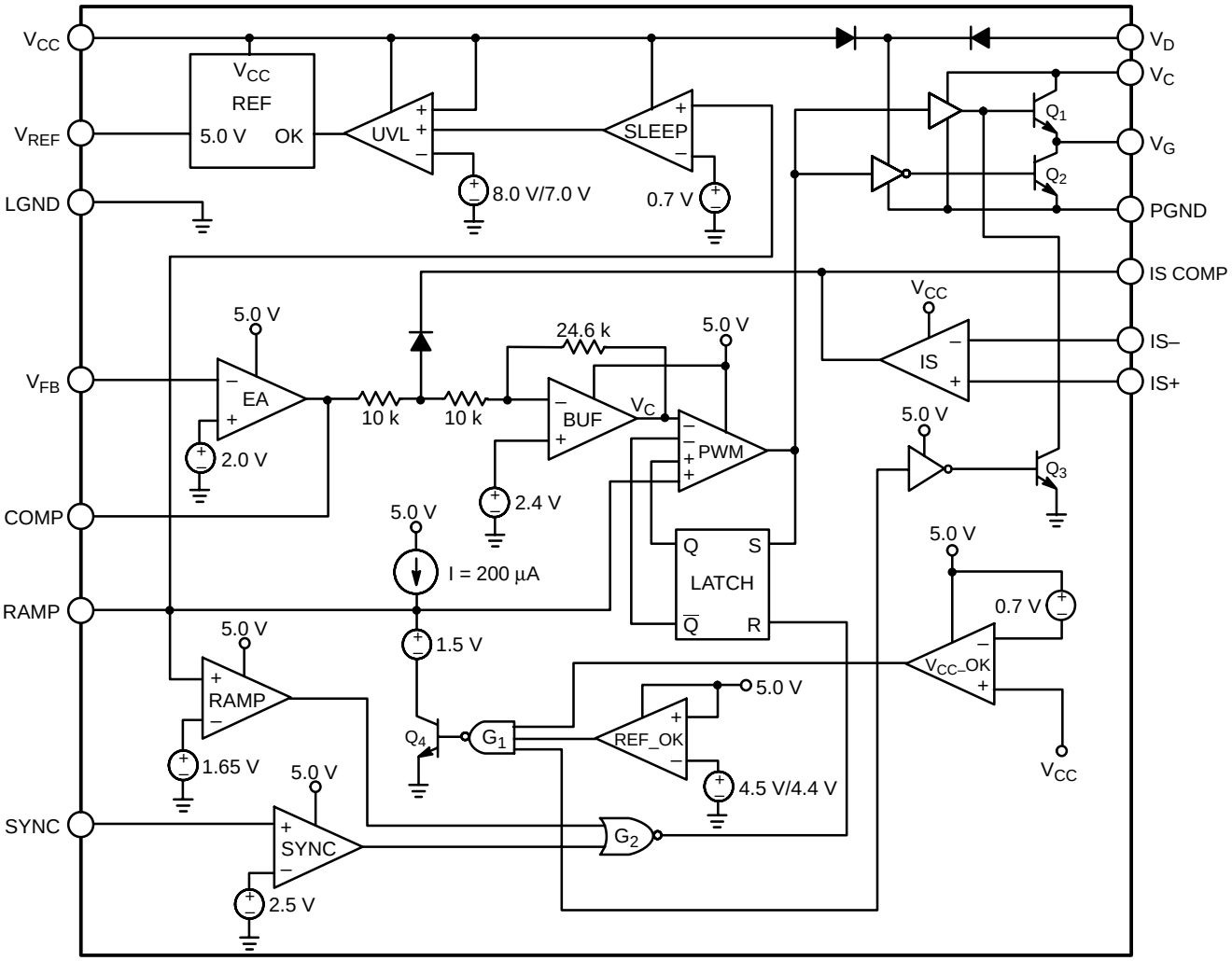

Figure 6. CS5101 Block Diagram

If the RAMP pin voltage is pulled below 0.7 V, the controller goes into a sleep mode where the output is disabled and the quiescent current is reduced.

Connecting the SSPR in a Circuit

The SSPR can be used in a variety of topologies including both single and dual ended buck or flyback converters operating with current or voltage mode control.

In each case, usually the N–FET power switch is connected in series with the forward diode as shown in Figure 7.

Since the N–FET is connected between two diodes it is impossible to use a single package center–tap rectifier. The source voltage of the N–FET changes from the secondary side peak voltage to approximately –0.7 V (the flyback diode forward drop) so the user must create a floating gate drive.

If it is not necessary to have a common ground connection between all outputs on the secondary side, the inductor can be connected on the ground side as shown in Figure 8.

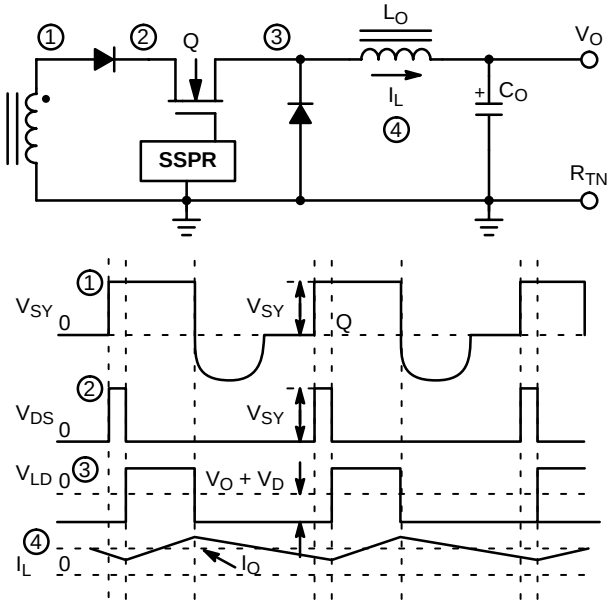

Figure 7. Primary Switch Current Waveforms

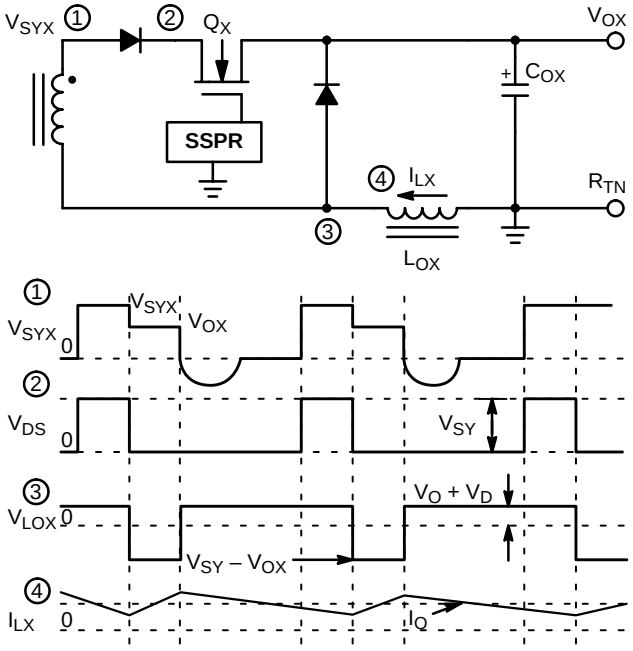

Figure 8. SSPR Connected in the Return

In this configuration the source of the N–FET is effectively a DC voltage, equal to the output voltage V_O. This makes the gate drive circuit for the FET simple and reliable. The V_C and V_{CC} voltages can be derived from the same point. Because the positive voltage transition across the inductor is clamped by the output voltage it may be necessary to generate the SYNC pulse from another secondary output.

There are two ways to generate a negative output voltage. One way is simply to reverse the ground and output connections as is shown in Figure 9. The SSPR circuit is referenced to the negative output.

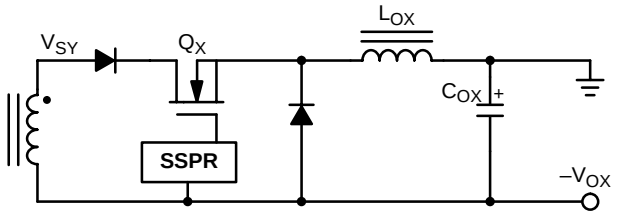

Figure 9. SSPR for Negative Output

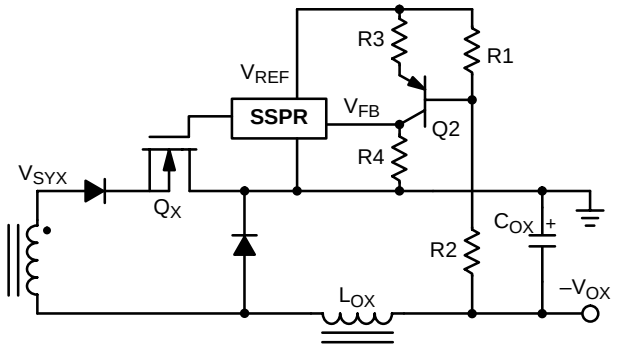

Figure 10. Ground Referenced Negative Output SSPR

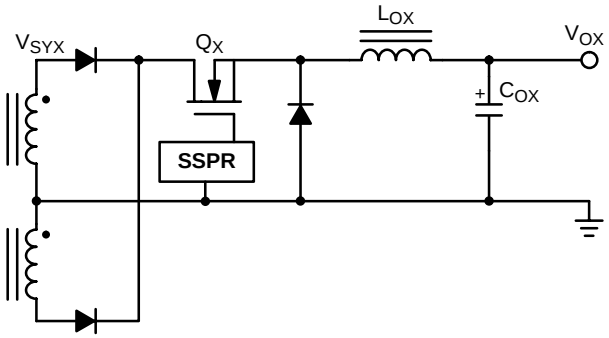

Figure 11. Dual Ended SSPR

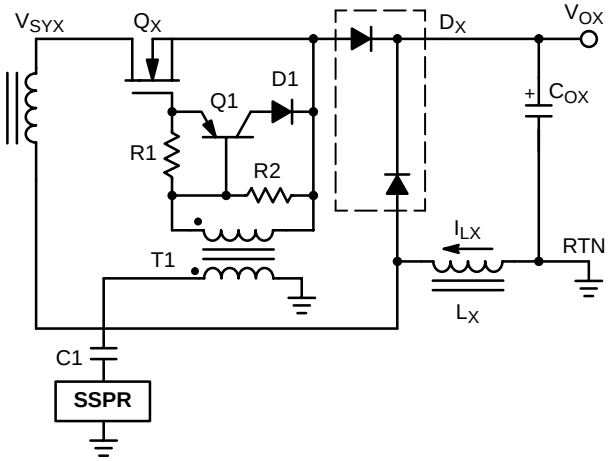

Figure 12. SSPR with Gate Drive Transformer

Another method is shown in Figure 10. The SSPR gate drive circuit is referenced to ground. An additional feedback signal inversion is required in this case.

With dual ended topologies such as a push–pull or bridge, only one power switch is required to control the output voltage. The output inductor can be connected in either the positive or return path. The SSPR should switch at twice the rate of the primary controller.

For the high power application, when a single package center–tapped rectifier is required, SSPR power switch can be driven by the gate drive transformer as shown in Figure 12.

Design Example

As an example, we show the design of a dual output current mode control forward converter. The 5.0 V output is controlled by the main loop with feedback connected to the primary side PWM controller (CS3842A). The second 3.3 V output is controlled by the CS5101.

Design Specifications

Input Voltage Range . . . . . 18 to 36 V_{DC}
Output Voltage, VO1 . . . . . 5.0 V_{DC}
Output Voltage, VO2 . . . . . 3.3 V_{DC}
Output Current, IO1 . . . . . 0.2 to 3.0 A_{DC}
Output Current, IO2 . . . . . 0.3 to 2.0 A_{DC}

Switching Frequency . . . . . 100 kHz
Line/Load Regulation at all outputs 1.0%

1. Power Transformer Design

To leave enough head room for SSPR operation at high line, assume the duty cycle at low line, D_{LL} is 0.6.

Voltage at the 5.0 V winding:

$$V_{SY5} = \frac{5.0 + 0.6}{0.6} = 9.33\ V$$

Transformer turns ratio:

$$n = \frac{V_{SY}}{V_{PY}} = \frac{9.33}{18} = 0.518$$

Use TDK core PC40EER25.5 – Z.

Minimum number of primary turns:

$$N_{PY} = \frac{V_{IN(MIN)} \times t_{ON}}{B_m \times A_e} 10^8$$

where:

B_m = Flux Density, in Gauss;

A_e = Effective core cross section area, in cm^2;

t_{ON} = Power switch on–time at low line;

$V_{IN(MIN)}$ = Minimum input voltage.

Rewriting this equation, in terms of duty cycle, D, and switching frequency, $f_{SW,}$:

$$N_{PY} = \frac{V_{IN(MIN)} \times D_{MAX}}{f_{SW} \times B_m \times A_e} 10^8$$

$$N_{PY} = \frac{18 \times 0.6}{100\ k \times 1.2\ k \times 0.448} 10^8 = 20\ turns$$

Secondary turns for 5.0 V output:

$$N_{SY5} = 20 \times n = 20 \times 0.518 = 10.36\ turns$$

N_{SY5} = 11 T.

Use the same number of turns for both the 3.3 V and 5.0 V outputs. The turns ratio of the power transformer N_{PY}:N_{SY5}:N_{SY3}:N_{AUX} is equal to 20:11:11:8.

The transformer is reset with the clamp reset circuit comprising D8, R10, C18. At turn–off, the drain voltage of Q2 is clamped to a voltage equal to the input voltage plus the voltage across capacitor C18.

Actual duty cycle at low line:

$$D_{LL} = \frac{V_O + V_D}{V_{IN(MIN)} \times n}$$

$$D_{LL} = \frac{(5.0 + 0.8) \times 20}{18 \times 11} = 0.586$$

Duty cycle at high line:

$$D_{HL} = D_{LL} \times \frac{V_{IN(MIN)}}{V_{IN(MAX)}}$$

$$D_{HL} = 0.586 \times \frac{18}{36} = 0.293$$

Output Inductor Design

We must maintain continuous mode operation at minimum load and maximum input voltage conditions.

5.0 V Output Inductor, L1

$I_{O5(MIN)}$ = 0.25 A; D_{MIN} = 0.293; f_{SW} = 100 kHz;

$\Delta I = 2.0 \times I_{O(MIN)}$ = 0.5 A.

Rectifier diode forward drop V_D = 0.75 @ 3.0 A. (MBR360)

The output inductor is calculated with the following equation:

$$L_{MIN} = \frac{(V_O + V_D) \times t_{OFF(MAX)}}{\Delta I}$$

$$L_{MIN} = \frac{(5.0 + 0.75) \times (1.0 - 0.293)}{100\ k \times 0.5} = 81\ \mu H$$

Allowing for a 20% tolerance in the inductor, L1 = 100 μH.

Use a T72–26 Powdered Iron Core from Micrometals.

Winding data: 34T, #24AWG.

3.3 V Output Inductor, L2

$I_{O3(MIN)}$ = 0.3 A; ΔI = 0.6 A.

Using the equation for output inductor, determine L2.

$$L_{O3(MIN)} = \frac{(3.3 + 0.75) \times (1.0 - 0.293)}{100\ k \times 0.6} = 48\ \mu H$$

L2 = 50 μH.

Use a T80–26 Powdered Iron Core from Micrometals.

Winding data: 42T, #24AWG.

Use a 330 μF, 15 V Aluminum Electrolytic Capacitor with ESR = 0.12 Ω on both outputs.

Ripple due to the ESR on the 5.0 V output:

$$\Delta V_{O5} = 0.12 \times 0.5 = 60\ mV_{P-P}$$

Ripple due to the ESR on the 3.3 V output:

$$\Delta V_{O3} = 0.12 \times 0.6 = 72\ mV_{P-P}$$

Because the regulator uses current mode control, the primary side peak current is sensed across the current sense resistor, R10. This primary side current is the combination of currents from both outputs. The effective slope of the current in the primary side is influenced by both output inductors. The outputs are reflected to the main output based on the turns ratio. The combined equivalent circuit is shown in Figure 13.

Inductance and capacitance reflected from the 3.3 V output to the main output is given by:

$$L'_{O3} = \frac{L_{O3}}{n^2}$$

$$C'_{O3} = C_{O3} \times n^2$$

Voltage and current reflected from the 3.3 V output to the main output is given by:

$$V'_{O3} = \frac{V_{O3}}{n}$$

$$I'_{O3} = I_{O3} \times n$$

Reflected ESR is:

$$ESR'_{O3} = \frac{ESR_{O3}}{n^2}$$

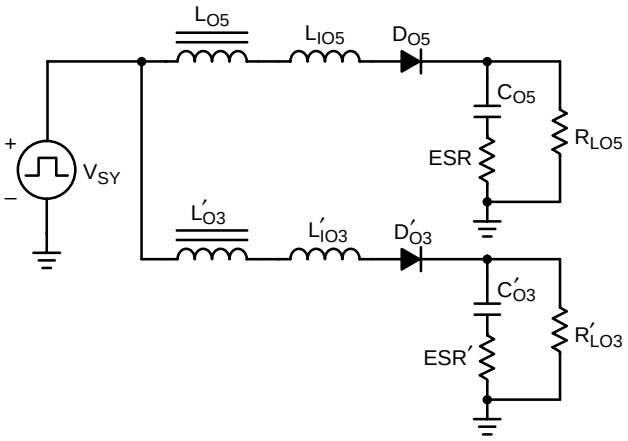

Figure 13. Secondary Side Normalized Current

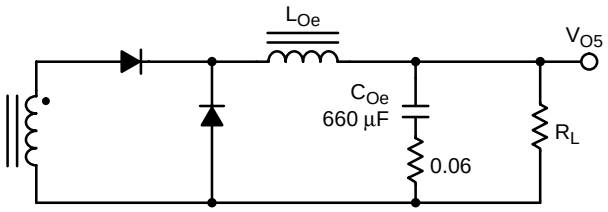

Figure 14. Main Output Equivalent Circuit

The turns ratio for the secondary windings is 1:1.

Then, effective inductance:

$$L_{Oe} = \frac{L_{O5} \times L'_{O3}}{L_{O5} + L'_{O3}}$$

$$L_{Oe} = \frac{100\ \mu \times 50\ \mu}{100\ \mu + 50\ \mu} = 33.3\ \mu H$$

Effective capacitance:

$$C_{Oe} = C'_{O3} + C_{O5} = 330 + 330 = 660\ \mu F$$

Slope Compensation

Because the duty cycle exceeds 50% at low input voltage, slope compensation is required to avoid instability.

Output inductor effective down slope, m_e is given by

$$m_e = \frac{I}{t} = \frac{V_L}{L_e} = \frac{5.0 + 0.75}{33.3\ \mu H} = 0.173\ V/\mu s$$

The recommended slope compensation is one half of m_e.

Due to the increased noise created by the SSPR at turn–on, the slope compensation should be increased to 0.6.

$$m_{COMP(SY)} = 0.7 \times m_e = 0.104\ V/\mu s$$

The compensation voltage, V_{COMP}, is given by:

$$V_{COMP} = \frac{m_{COMP(SY)} \times N_{SY}}{N_{PY}} \times R10$$

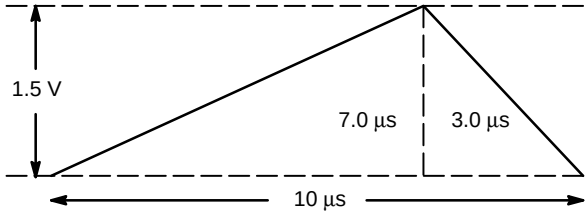

Figure 15. CS3842A Oscillator Voltage

$$V_{COMP} = \frac{0.104 \times 11}{20} \times 0.25 = 14.3 \times 10^{-3}\ V/\mu s$$

PWM controller oscillator slope (see Figure 15), ΔV_{OSC} = 1.7 V; Δt_{OSC} = 7.0 μs:

$$m_{OSC} = \frac{1.7}{7.0} = 0.243\ V/\mu s$$

$$R4 = \frac{R11 \times m_{OSC}}{m_{COMP}} = \frac{100 \times 0.243}{14.3 \times 10^{-3}} = 1.7\ k\Omega$$

Main Loop Compensation

Figure 16 shows the main components for loop compensation.

In general, for peak current mode control, the following expressions apply: $I_L = KV_C$ and $V_O = I_L R_L$, where $V_C = \Delta V_e$ (the error amplifier dynamic range).

For CS3842A, V_C = 2.5 V, and

$$V_O = K \times R_L \times \frac{V_C}{3.0}$$

From Figure 16,

$$K = \frac{N_{PY}}{N_{SY}} \times \frac{1.0}{R10}$$

Equivalent circuit for the output is shown in Figure 14.

L_{Oe} = 37.5 μH; C_{Oe} = 660 μF.

The output power range is:

$$P_{OMAX} = 5.0 \times 3.0 + 3.3 \times 2.0 = 21.6\ W$$

$$P_{OMIN} = 5.0 \times 0.25 = 1.25\ W$$

R_{LMAX} = 20 Ω; R_{LMIN} = 1.16 Ω.

Sliding pole:

$$f_P = \frac{1.0}{2.0\pi R_L C_O}$$

$$f_{PMIN} = \frac{1.0}{2.0\pi \times 20\ \Omega \times 660\ \mu F} = 12\ Hz$$

$$f_{PMAX} = \frac{1.0}{2.0\pi \times 1.16\ \Omega \times 660\ \mu F} = 208\ Hz$$

Output capacitor ESR zero:

$$f_Z = \frac{1.0}{2.0\pi(ESR)C_O} = \frac{1.0}{2.0\pi \times 0.06 \times 660\ \mu F} = 4.02\ kHz$$

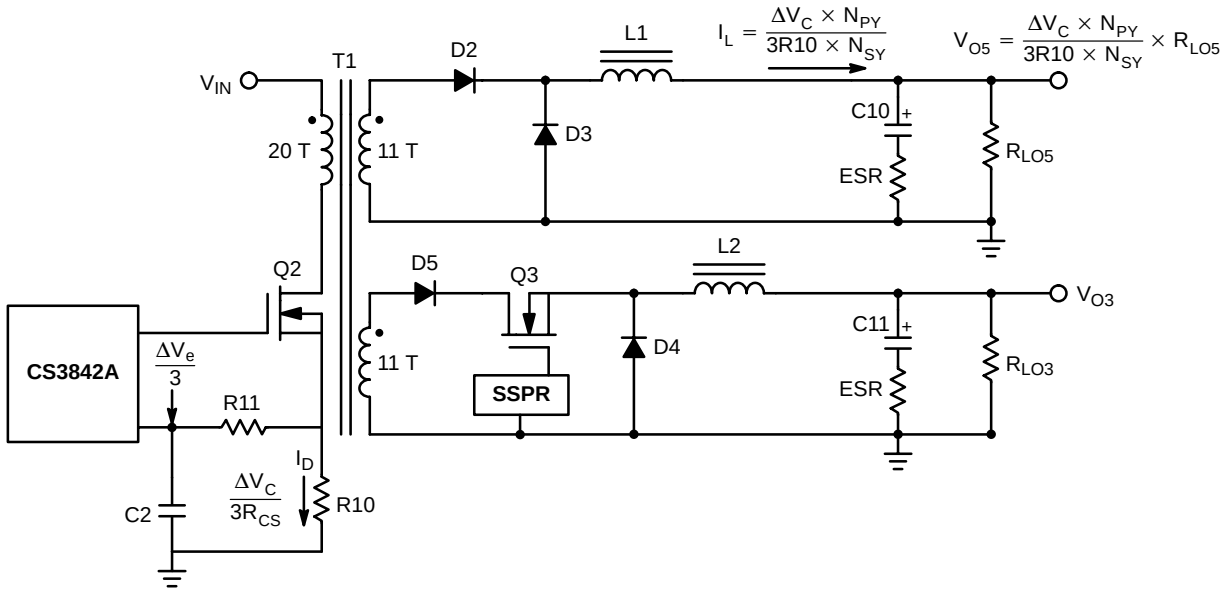

Figure 16. Main Loop Circuit

Control to output gain (see Figure 16):

$$G = \frac{dV_O}{dV_C} = \frac{N_{PY}}{N_{SY}} \times \frac{R_L}{3.0 \times R10}$$

Gain at high line:

$$G_{HL} = \frac{20}{11} \times \frac{20}{3.0 \times 0.25} = 48.5\ (33.7\ dB)$$

Gain at low line:

$$G_{LL} = \frac{20}{11} \times \frac{1.16}{3.0 \times 0.25} = 2.81\ (9.0\ dB)$$

It is good practice to make the crossover frequency between f_P (pole at high load) and f_{ZESR} (zero of output capacitor), i.e., $f_{CO} = 3.0$ kHz

Error amplifier gain needed to cross at 3.0 kHz:

$$G_{3.0\ kHz} = G_{HL} - 20 \log \frac{f_{CO}}{f_{PMIN}}$$

$$G_{3.0\ kHz} = 33.7 - 20 \log \frac{3.0\ K}{12} = 14.2\ dB\ (5.13\ times)$$

The error amplifier feedback resistor, R3, is equal to:

$$R3 = 5.13 \times R1 = 5.13 \times 4.99\ k\Omega = 25.5\ k\Omega$$

Pole to cancel the ESR zero: $f_{PESR} = f_{ZESR} = 4.02$ kHz, then

$$C1 = \frac{1.0}{2.0\pi \times 4.02\ kHz \times 25.5\ k\Omega} = 1.5\ nF$$

Another zero is placed at low frequency: $f_{Z1} = f_{PMIN} = 12$ Hz, then

$$C13 = \frac{1.0}{2.0\pi \times 12 \times 25.5\ k\Omega} = 520 \times 10^{-9} = 0.47\ \mu F$$

The frequency response diagram of the main loop is shown in Figure 17.

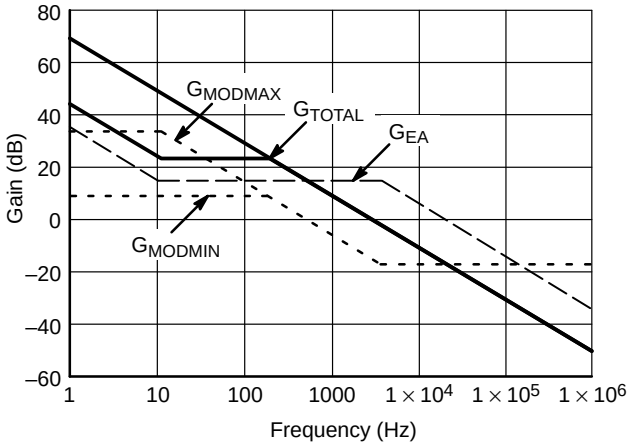

Figure 17. Main Loop Frequency Characteristics

The loop crossover frequency is 3.0 kHz with an adequate phase margin.

SSPR Controlled Output Calculation

The following data from the specification and the previous calculations are important for the design.

Switching frequency: 100 kHz;

Transfer turns ratio: N_{PY}:N_{O5}:N_{O3} = 20:11:11;

Input voltage range: 18 to 36 V_{DC};

Duty cycle range determined by the 5.0 V output, $D_{MAX} = 0.586$, $D_{MIN} = 0.293$;

$L_{O3} = 50\ \mu H$;

$C_{O3} = 330\ \mu F$;

ESR = 0.12 Ω;

Voltage at the 3.3V winding at low line:V_{SY3} = 18(11/20) = 9.90 V.

Assuming the Schottky rectifier forward drop is 0.75 V and the DC voltage drop across the FET plus the winding resistance is 0.1 V at full load, the duty cycle required to maintain regulation:

$$D_{O3LL} = \frac{3.3 + 0.75 + 0.1}{9.9} = 0.419$$

$$D_{O3HL} = \frac{3.3 + 0.75 + 0.1}{19.8} = 0.209$$

The difference between the actual duty cycle and required, is calculated at high line;

$$\Delta D_{O3HL} = 0.293 - 0.209 = 0.084$$

For 100 kHz, switching frequency

$$\Delta t_{O3HL} = 10\ \mu s \times 0.084 = 840\ ns$$

The delay time through the SSPR is typically 300 ns, leaving enough head room for a good regulation within the specified voltage range.

Supply Voltage V_{CC} and V_C

The supply voltage is derived directly from the 3.3 V winding. V_{CC} varies with the input voltage, i.e., V_{CC} = 9.0 V to 19 V.

V_{CC} is referenced to ground while the gate drive voltage, V_C is bootstrapped and referenced to the source of Q3, i.e., V_C = 8.0 V to 18 V.

Synchronization Voltage

The synchronization voltage threshold of the CS5101 is 2.5 V. For reliable operation, the voltage at the SYNC pin has to be higher than 2.5 V at all times during the pulse.

Voltage at SYNC pin:

$$V_{SYNC(MIN)} = V_{SY(MIN)} \frac{R14}{R13 + R14}$$

$$V_{SYNC(MIN)} = \frac{18 \times 11}{20} \times \frac{15\ k}{5.1\ k + 15\ k} = 7.39\ V$$

$$V_{SYNC(MAX)} = \frac{36 \times 11}{20} \times \frac{15\ k}{5.1\ k} = 14.87\ V$$

Since the voltage at the winding is negative during the reset time, a clamp diode, D9, is placed across R14. A small capacitor C15, helps to reduce the negative going voltage spike at the turn–on of the power switch. This spike is due to the leakage inductance between primary and secondary windings.

Ramp Capacitor

The value of the ramp capacitor is calculated using the minimum on–time (at high line), and the current from the internal current source.

Ramp dynamic range:

$$\Delta V_R = 3.5 - 1.5 = 2.0\ V$$

Minimum pulse duration at 36 V input voltage:

$$t_{ON(MIN)} = \frac{D_{MIN}}{f_{SW}} = \frac{0.293}{100\ kHz} = 2.93\ \mu s$$

The goal is, during the pulse, to charge the ramp capacitor C_{RAMP} to a peak voltage.

Ramp charge current, I_{CHARGE} = 0.2 mA.

$$C_{RAMP} = \frac{I_{CHARGE} t_{ON(MIN)}}{\Delta V_R}$$

$$C_{RAMP} = \frac{0.2\ mA \times 0.293\ \mu s}{2.0\ V} = 293 \times 10^{-12}$$

C_{RAMP} = C16 = 300 pF.

Drain Resistor

A small current is needed to keep the output stage in a low impedance state during abnormal or shutdown conditions. Drain pin current should be checked at the extremes of the supply voltage.

$$I_{DMAX} = \frac{19.8\ V}{10\ k\Omega} = 1.98\ mA$$

$$I_{DMIN} = \frac{9.9\ V}{10\ k\Omega} = 0.99\ mA$$

Overcurrent Protection

Output current is sensed by the current sense resistor, R19, in the return path of the output. A voltage divider, comprised of resistors R16, R17, R20, and R21, is connected to the current sense amplifier. It is capable of sensing voltages below ground, up to 0.3 V.

Overcurrent protection is set to: I_{SCO3} = 25 A; R_{CS} = R19 = 0.1 Ω.

Current sense voltage:

$$V_{CS} = 2.5 \times 0.1 = 0.25\ V$$

Both dividers are connected to the 5.0 V reference voltage, provided by the CS5101.

Set current through the dividers to 0.5 mA. The voltage at IS– pin (inverting input) is set to 2.5 V, so R17 = R20 = 5.11 k.

The values of resistors R16 and R21, connected to IS+ (non–inverting input) are calculated using superposition.

$$V'_{IS+} = V_{REF} \frac{R21 + R19}{R16 + R21 + R19}\ \text{(zero load current)}$$

$$V''_{IS+} = V_{CS} \frac{R16}{R16 + R21 + R19}\ (V_{REF}\ \text{is shorted})$$

Since R19 is small, it is ignored.

$$V_{IS+} = V'_{IS+} - V''_{IS+}$$

$$= V_{REF} \frac{R21}{R16 + R21} - V_{CS} \frac{R16}{R16 + R21}$$

At trip point,

$$V_{IS+} = V_{IS-} = 2.5\ V$$

$$R16 + R21 = 10\ k\Omega,\ \text{then}$$

$$2.5 = 5 \times \frac{R21}{10\ k\Omega} - 0.25 \times \frac{R16}{10\ k\Omega}$$

$$R16 = 10\ k\Omega - R21$$

Substituting R21 = 5.23 kΩ, R16 = 4.75 kΩ.

With C22 = 0.22 μF, current sense amplifier crossover frequency is:

$$f_{CSO} = \frac{1}{2\pi \times R17 \times C22}$$

$$f_{CSO} = \frac{1}{2\pi \times 5.11\ k\Omega \times 0.22\ \mu F} = 142\ Hz$$

SSPR Loop Compensation

The SSPR operates in voltage control mode. The control loop model is shown in Figure 18.

The modulator gain varies with input voltage, and from ref [3] is:

$$G_m = \frac{DV_O}{DV_C} = \frac{-V_{SY}}{\Delta V_C} He(s)$$

He(s) is represented by the double pole of the output filter and zero of the output capacitor's ESR, i.e.,

$$f_P = \frac{1}{2\pi\sqrt{L_2 C_{11}}};\ f_Z = \frac{1}{2\pi C_{11} ESR}$$

Modulator gain at input voltage extremes:

$$G_{O3(MAX)} = \frac{19.8}{2.5} = 7.92\ (17.97\ dB)$$

$$G_{O3(MIN)} = \frac{9.9}{2.5} = 3.96\ (11.95\ dB)$$

$$f_{PO3} = \frac{1}{2\pi\sqrt{50\ \mu H \times 330\ \mu F}} = 1.24\ kHz$$

$$f_{ZO3} = \frac{1}{2\pi \times 0.12\ \Omega \times 330\ \mu F} = 4.02\ kHz$$

Crossover frequencies:

$$f_{CO1} = 1.24 \times 10^{(11.95/40)} = 2.47\ kHz$$

$$f_{CO2} = 1.24 \times 10^{(17.97/40)} = 3.49\ kHz$$

Because of the interactions between the main loop and the loop controlled by the SSPR, it is recommended that the SSPR crossover frequency is at least one decade below the crossover frequency of the main loop (3.0 kHz, in our case). A simple single pole compensation is used.

The interaction is especially severe with current mode control at light load because of the high impedance of the driving source ref [2].

Techniques to reduce these effects are outlined in ref [4].

$$f_{CO3} = \frac{1}{2\pi \times C17 \times R25}$$

$$f_{CO3} = \frac{1}{2\pi \times 0.1\ \mu F \times 43\ k\Omega} = 122\ Hz$$

In general, voltage mode control with feed forward gives the best result for this type of application.

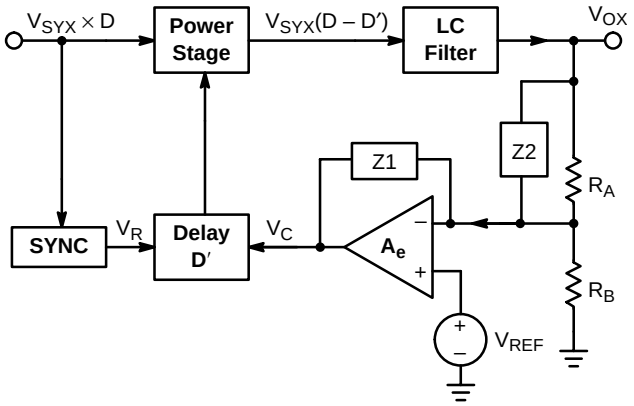

Figure 18. Modular Gain Block Diagram

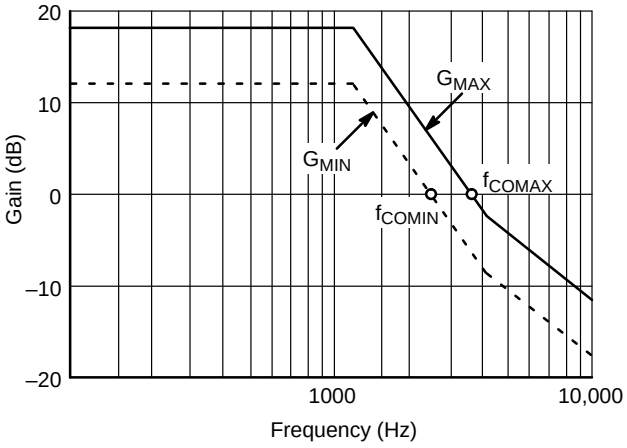

Figure 19. SSPR Loop Frequency Characteristics

Performance Results and Waveforms

The complete schematic, component placement and PC board layout are shown in Figures 22 through 25.

The electrical performance characteristics of the demo board are shown in Table 1.

The load and line regulation of the 3.3 V output is better than 0.3%.

Actual waveforms of the demo board are shown in Figures 20 and 21.

Table 1. Demo Board Performance Measurements

	Main Output		SSPR Output	
V_{IN}	Current	Voltage	Current	Voltage
18 V	0.25 A	5.04	0 A	3.273
18 V	0.25 A	5.04	2.25 A	3.268
18 V	3.0 A	5.04	0 A	3.274
18 V	3.0 A	5.04	2.25 A	3.269
36 V	0.25 A	5.05	0 A	3.277
36 V	0.25 A	5.04	2.25 A	3.272
36 V	3.0 A	5.04	2.25 A	3.276
36 V	3.0 A	5.04	2.25 A	3.272

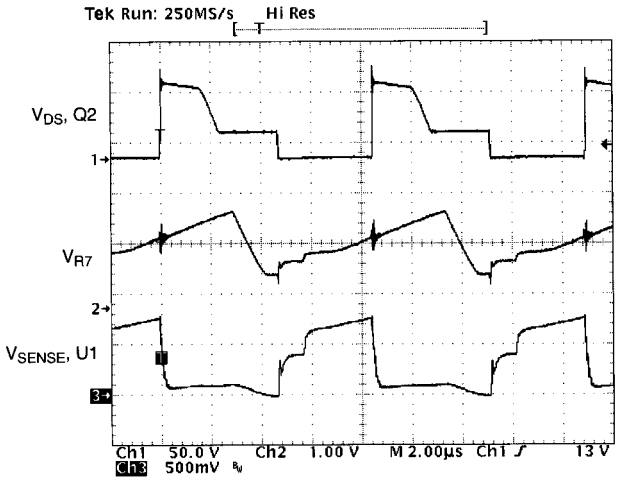

Figure 20. Primary Side Waveforms

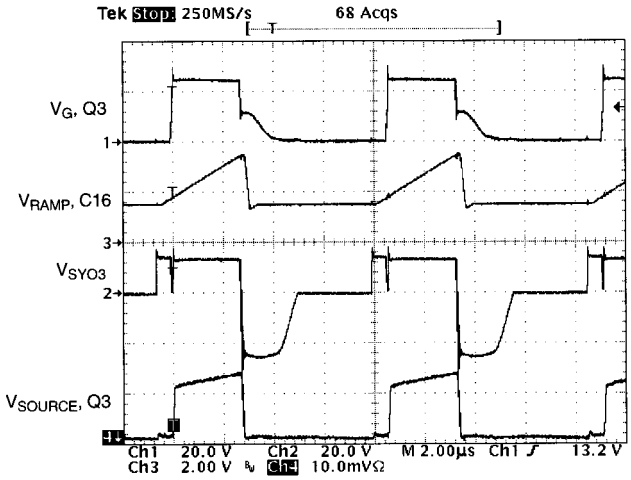

Figure 21. SSPR Waveforms

Special thanks to Kieran O'Malley for his help, and Bob Kent and German Martinez for their significant contributions to the development of the demo board.

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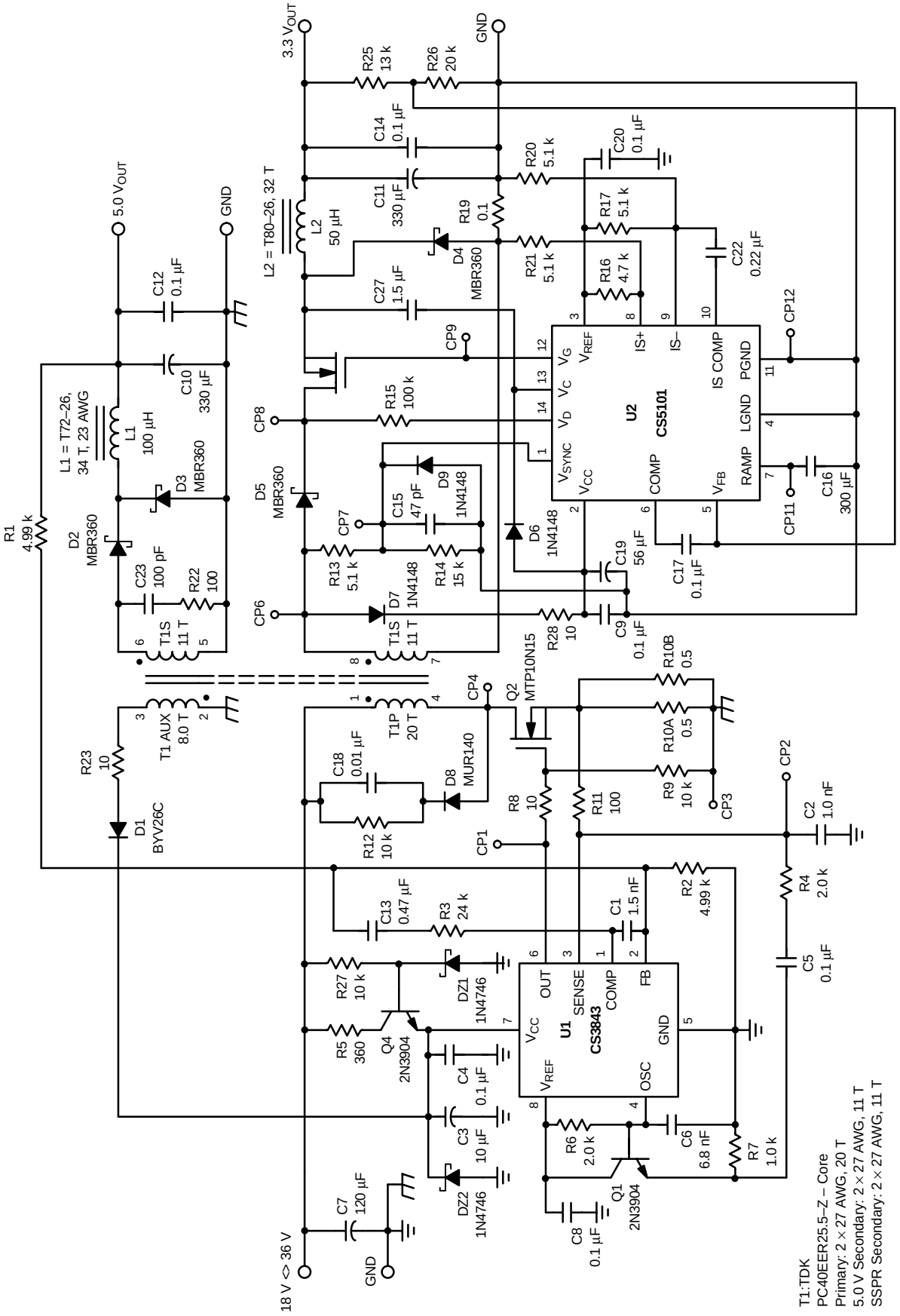

Figure 22. Forward Converter with SSPR Controlled Output

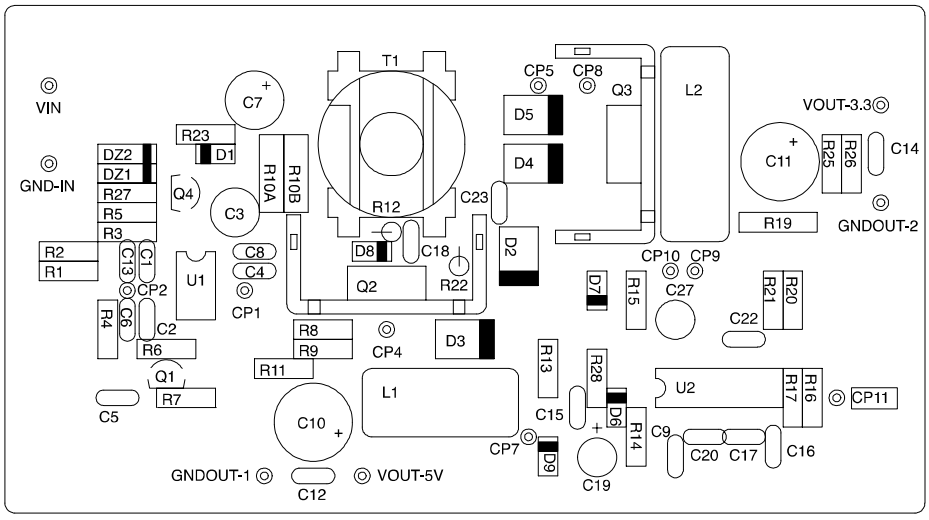

Figure 23. Component Placement

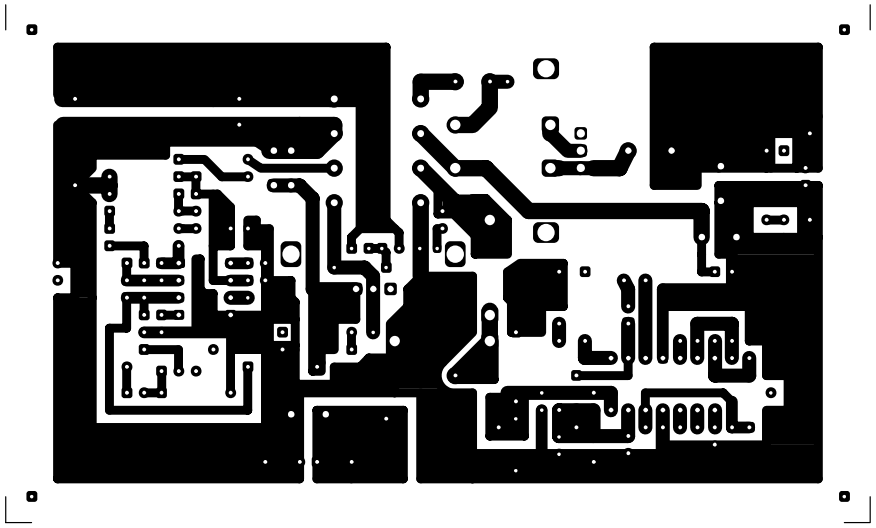

Figure 24. Bottom Metal Layer

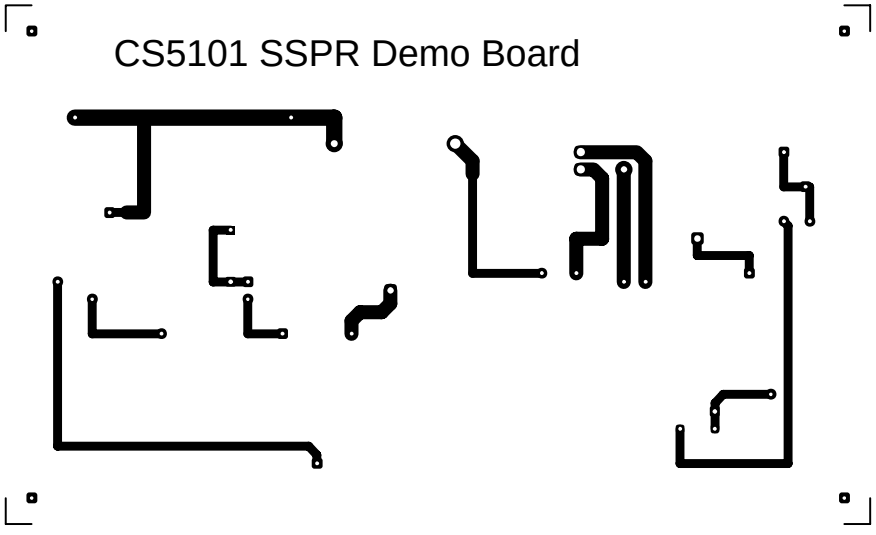

Figure 25. Top Metal Layer

Table 2. Parts List of Discrete Components

Qty	Type	Value	Designator	Manufacturer	Distributor	Part #
1	Monolithic	47 pF	C15	Panasonic	Digi–Key	P4845–ND
1	Monolithic	100 pF	C23	Panasonic	Digi–Key	P4800–ND
1	Monolithic	330 pF	C16	Panasonic	Digi–Key	P4806–ND
1	Monolithic	1.0 nF	C2	Panasonic	Digi–Key	P4812–ND
1	Monolithic	1.5 nF	C1	Panasonic	Digi–Key	P4814–ND
1	Monolithic	6.8 nF	C6	Panasonic	Digi–Key	P4880–ND
2	Monolithic	10 nF	C18, C21	Panasonic	Digi–Key	P4881–ND
8	Monolithic	0.1 μF	C4, C5, C8, C9, C12, C14, C17, C20	Panasonic	Digi–Key	P4887–ND
1	Monolithic	0.22 μF	C22	Panasonic	Digi–Key	P4889–ND
1	Monolithic	0.47 μF	C13	Panasonic	Digi–Key	P4891–ND
1	Tant/25 V	1.5 μF	C27	Panasonic	Digi–Key	P2044–ND
1	Tant/25 V	10 μF	C3	Panasonic	Digi–Key	P2049–ND
1	Electro/25 V	56 μF	C19	Panasonic	Digi–Key	P5696–ND
1	Electro/50 V	120 μF	C7	Panasonic	Digi–Key	P5764–ND
2	Electro/16 V	330 μF	C10, C11	Panasonic	Digi–Key	P5670–ND
1	Metal Film	0.1	R19	Caddock	Allied	524–6010
2	Metal Film	0.5	R10A, R10B	Caddock	Allied	524–6015
3	5.0%, 1/4 W	10	R8, R23, R28	Yageo	Digi–Key	10QBK–ND
2	5.0%, 1/4 W	100	R11, R22	Yageo	Digi–Key	100QBK–ND
1	5.0%, 1/4 W	360	R5	Yageo	Digi–Key	360QBK–ND
1	5.0%, 1/4 W	1.0 k	R7	Yageo	Digi–Key	1KQBK–ND
2	5.0%, 1/4 W	2.0 k	R4, R6	Yageo	Digi–Key	2KQBK–ND
1	5.0%, 1/4 W	4.7 k	R16	Yageo	Digi–Key	4.7KQBK–ND
2	1.0%, 1/4 W	4.99 k	R1, R2	Yageo	Digi–Key	4.99KXBK–ND
4	5.0%, 1/4 W	5.1 k	R13, R17, R20, R21	Yageo	Digi–Key	5.1KQBK–ND
3	5.0%, 1/4 W	10 k	R9, R12, R27	Yageo	Digi–Key	10KQBK–ND
1	5.0%, 1/4 W	100 k	R15	Yageo	Digi–Key	10KQBK–ND
1	5.0%, 1/4 W	13 k	R25	Yageo	Digi–Key	13KQBK–ND
1	5.0%, 1/4 W	15 k	R14	Yageo	Digi–Key	15KQBK–ND
1	5.0%, 1/4 W	20 k	R26	Yageo	Digi–Key	20KQBK–ND
1	5.0%, 1/4 W	24 k	R3	Yageo	Digi–Key	24KQBK–ND
2	MUR140	UFRD	D1, D8	Motorola	Newark	MUR140
2	1n4148	Diode	D6, D7	DIODES	Digi–Key	1N4148CT–ND
2	1n4744	18 V Zener	DZ1, DZ2	ITT	Digi–Key	1N4746ACT–ND
4	MBR360	30 V, 6.0 A Scht	D2, D3, D4, D5	Motorola	Newark	MBR360
2	2n3904	NPN	Q1, Q4	National	Digi–Key	2N3904–ND
2	MTP10N15	MOSFET–N	Q2, Q3	Motorola	Newark	MTP10N15
2	Heat Sinks	TO–220	HS1, HS2	Aavid	Digi–Key	HS120–ND

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